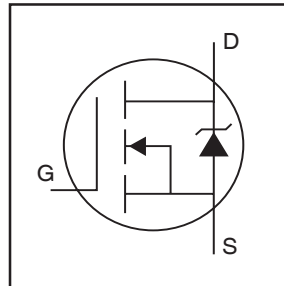


# IRFIZ48NPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

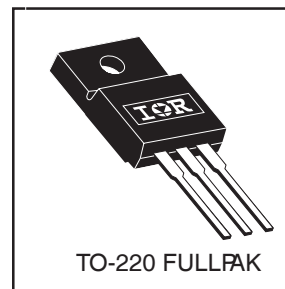


$V_{DSS} = 55V$
$R_{DS(on)} = 0.016\Omega$
$I_D = 40A$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	40	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	29	
$I_{DM}$	Pulsed Drain Current ①⑥	210	
$P_D @ T_C = 25^\circ C$	Power Dissipation	54	W
	Linear Derating Factor	0.36	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑥	270	mJ
$I_{AR}$	Avalanche Current①⑥	32	A
$E_{AR}$	Repetitive Avalanche Energy①	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

## Thermal Resistance

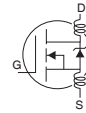
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	2.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient	---	65	

# IRFIZ48NPbF



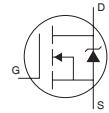
## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA④
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.016	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 22A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	22	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 32A⑥
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	89	nC	I <sub>D</sub> = 32A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	20		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	39		V <sub>GS</sub> = 10V, See Fig. 6 and 13 ④⑥
t <sub>d(on)</sub>	Turn-On Delay Time	—	11	—	ns	V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	78	—		I <sub>D</sub> = 32A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	32	—		R <sub>G</sub> = 5.1Ω
t <sub>f</sub>	Fall Time	—	48	—		R <sub>D</sub> = 0.85Ω, See Fig. 10 ④⑥
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	1900	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	620	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	270	—		f = 1.0MHz, See Fig. 5⑥
C	Drain to Sink Capacitance	—	12	—		f = 1.0MHz



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	49	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	210		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 22A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	94	140	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 32A
Q <sub>rr</sub>	Reverse Recovery Charge	—	360	540	nC	di/dt = 100A/μs ④⑥

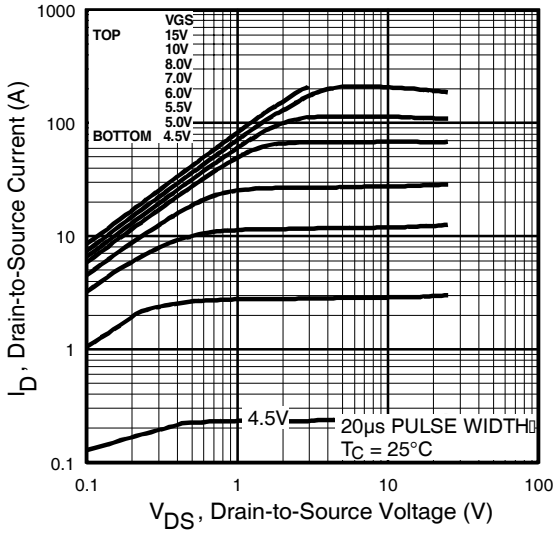


### Notes:

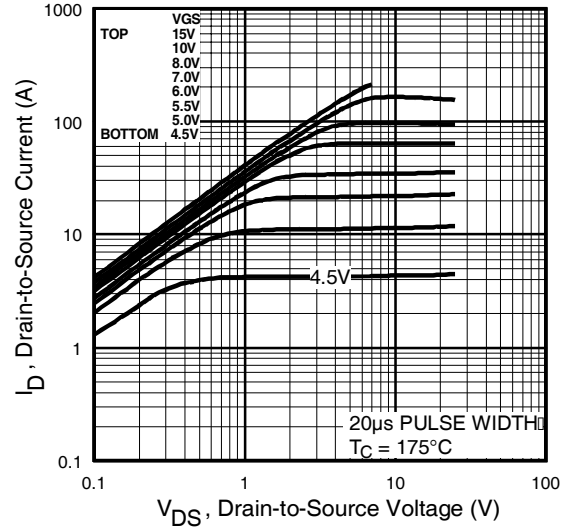
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 530μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 32A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 32A, di/dt ≤ 250A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ t = 60s, f = 60Hz
- ⑥ Uses IRFZ48N data and test conditions



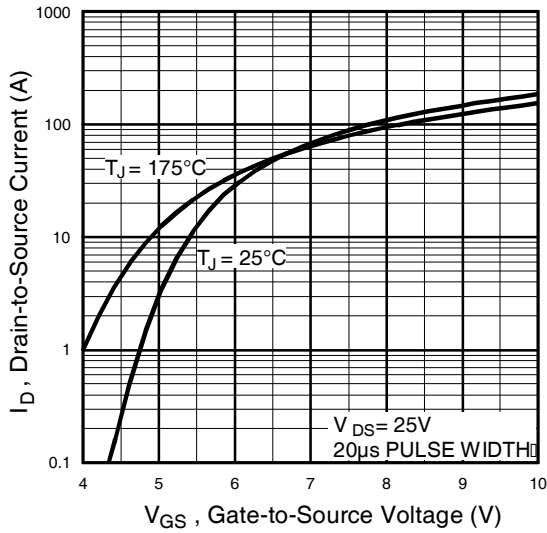
# IRFIZ48NPbF



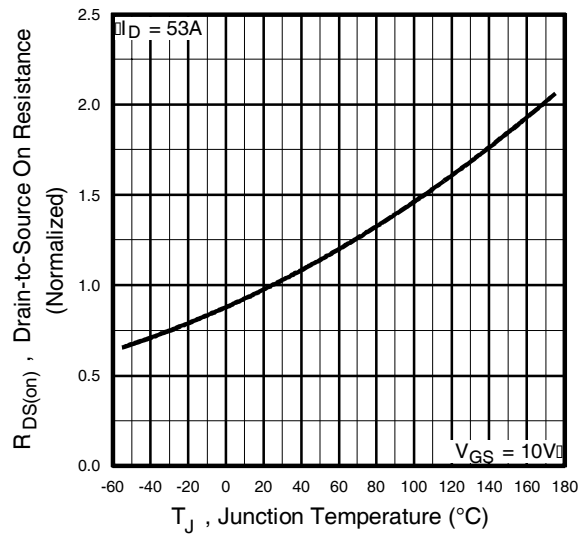
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

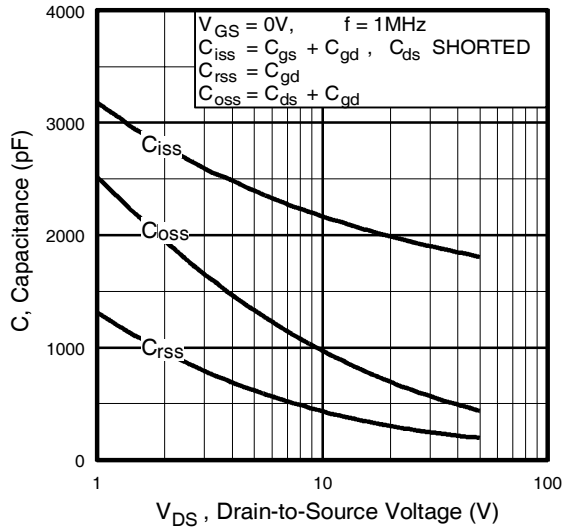


**Fig 3.** Typical Transfer Characteristics

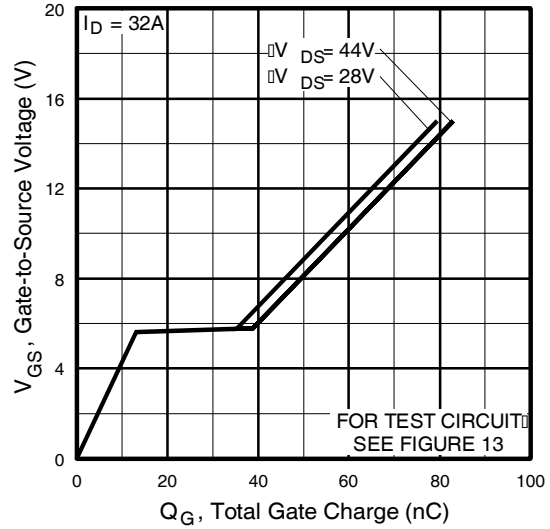


**Fig 4.** Normalized On-Resistance Vs. Temperature

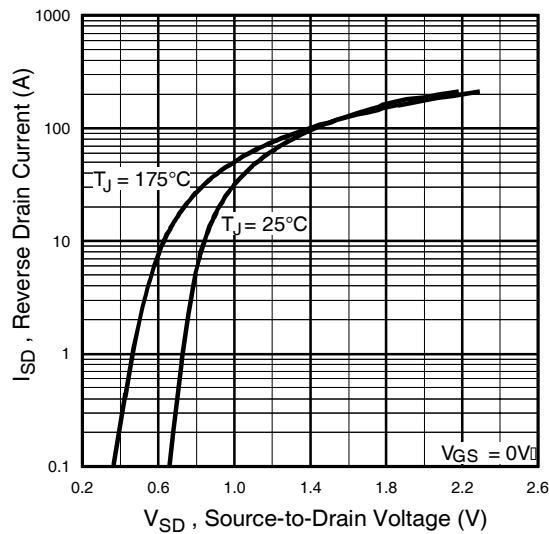
# IRFIZ48NPbF



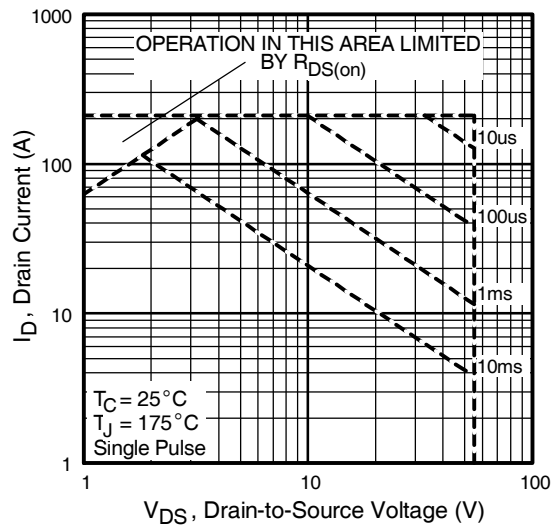
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



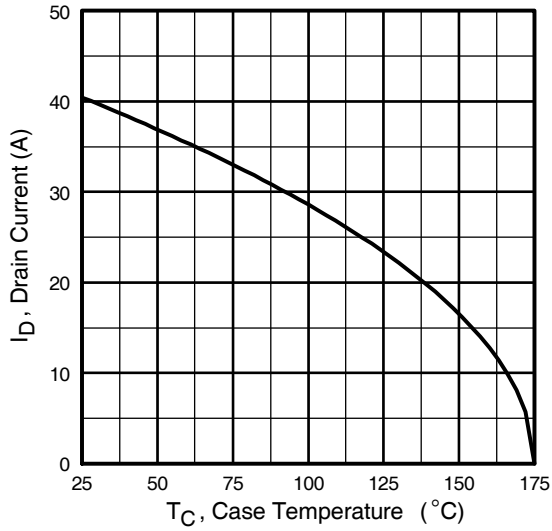
**Fig 7.** Typical Source-Drain Diode Forward Voltage



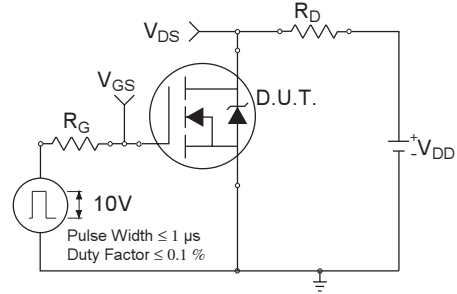
**Fig 8.** Maximum Safe Operating Area



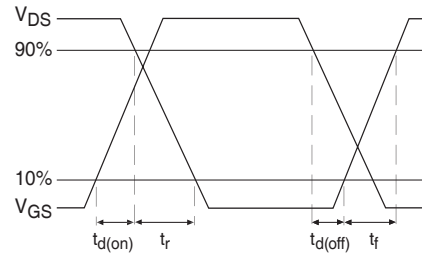
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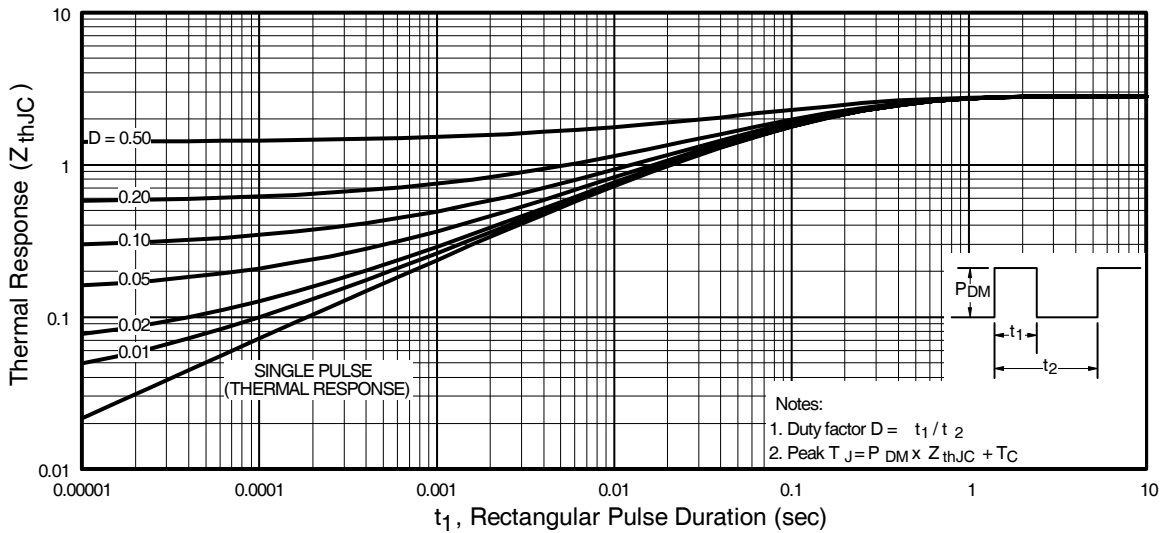
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

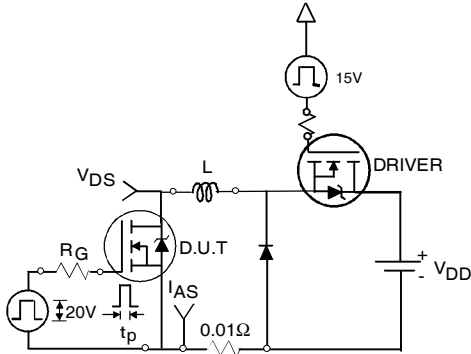


**Fig 10b.** Switching Time Waveforms

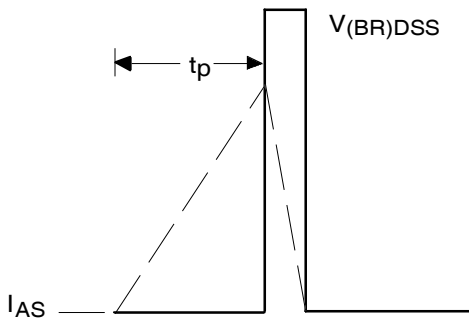


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

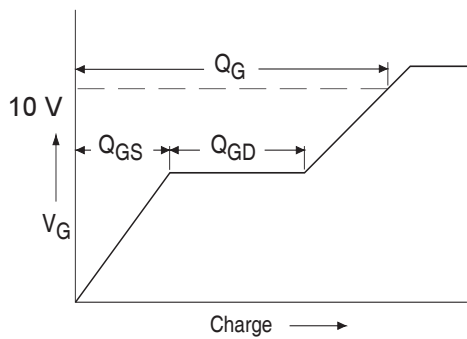
# IRFIZ48NPbF



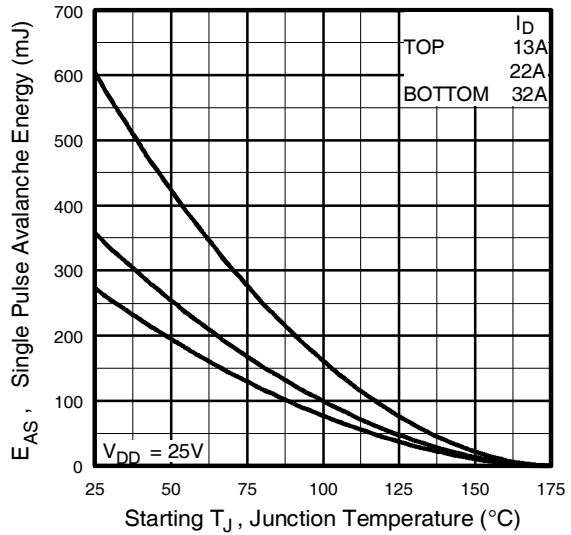
**Fig 12a.** Unclamped Inductive Test Circuit



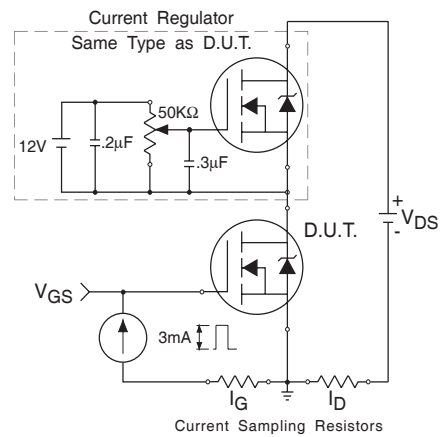
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

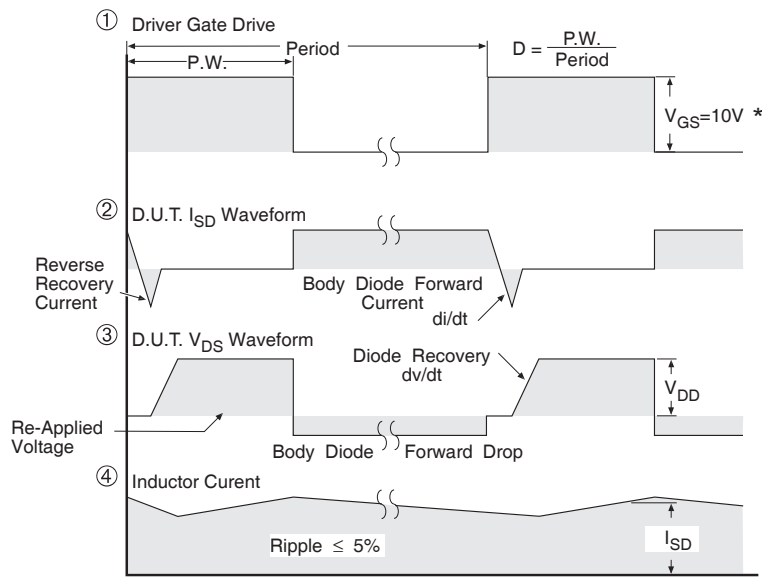


**Fig 13b.** Gate Charge Test Circuit



# IRFIZ48NPbF

## Peak Diode Recovery dv/dt Test Circuit



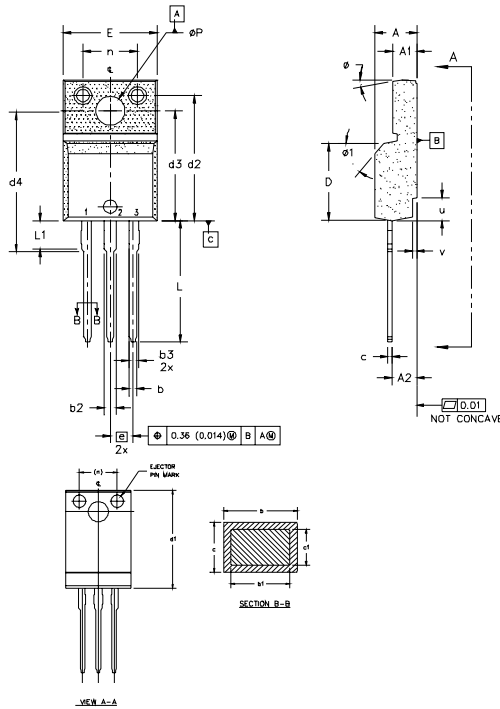
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

# IRFIZ48NPbF



## TO-220 Full-Pak Package Outline



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
  - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
  - 7.0 CONTROLLING DIMENSION : INCHES.

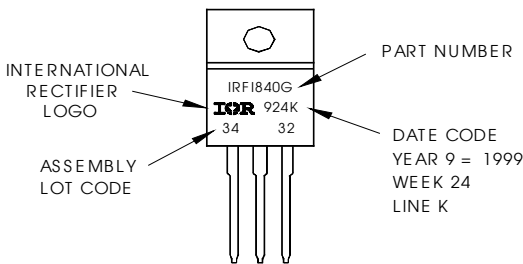
SYMBOL	DIMENSIONS		DIMENSIONS		NOTES
	MILLIMETERS	MILLIMETERS	INCHES	INCHES	
A	4.57	4.83	0.180	0.190	5
A1	2.57	2.85	0.101	0.114	
A2	2.51	2.85	0.099	0.112	
b	0.622	0.89	0.024	0.035	4
b1	0.622	0.838	0.024	0.033	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	4
c	0.440	0.629	0.017	0.025	
c1	0.440	0.584	0.017	0.023	
D	8.65	9.80	0.341	0.386	3
d1	15.80	16.12	0.622	0.635	
d2	13.97	14.22	0.550	0.560	
d3	12.30	12.92	0.484	0.509	4
d4	8.64	9.91	0.340	0.390	
E	10.35	10.63	0.408	0.419	
e	2.54 BSC		0.100 BSC		3
L	13.20	13.73	0.520	0.541	
L1	3.10	3.90	0.122	0.138	
n	6.05	6.15	0.238	0.242	6
p	3.05	3.45	0.120	0.136	
u	2.40	2.50	0.094	0.098	
v	0.40	0.50	0.016	0.020	6
w	3"	7"	3"	7"	
x1	45°	45°	45°	45°	

- LEAD ASSIGNMENTS
- HEXFET
- 1- GATE
  - 2- DRAIN
  - 3- SOURCE
- IGBTs, CoPACK
- 1- GATE
  - 2- COLLECTOR
  - 3- EMITTER

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G  
 WITH ASSEMBLY  
 LOT CODE 3432  
 ASSEMBLED ON WW 24 1999  
 IN THE ASSEMBLY LINE "K"

**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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 TAC Fax: (310) 252-7903  
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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

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