LM2937-2.5, LM2937-3.3 400mA and 500mA Voltage Regulators

Check for Samples: LM2937-2.5, LM2937-3.3

FEATURES

- **Fully Specified for Operation Over −40°C to +125°C**
- **Output Current in Excess of 500 mA (400mA for SOT-223 package)**
- **Output Trimmed for 5% Tolerance Under All Operating Conditions**
- **Wide Output Capacitor ESR Range, 0.01Ω up to 5Ω**
- **Internal Short Circuit and Thermal Overload Protection**
- **Reverse Battery Protection**
- **60V Input Transient Protection**
- **Mirror Image Insertion Protection**

DESCRIPTION

The LM2937-2.5 and LM2937-3.3 are positive voltage regulators capable of supplying up to 500 mA of load current. Both regulators are ideal for converting a common 5V logic supply, or higher input supply voltage, to the lower 2.5V and 3.3V supplies to power VLSI ASIC's and microcontrollers. Special circuitry has been incorporated to minimize the quiescent current to typically only 10 mA with a full 500 mA load current when the input to output voltage differential is greater than 5V.

The LM2937 requires an output bypass capacitor for stability. As with most regulators utilizing a PNP pass transistor, the ESR of this capacitor remains a critical design parameter, but the LM2937-2.5 and LM2937-3.3 include special compensation circuitry that relaxes ESR requirements. The LM2937 is stable for all ESR ratings less than 5Ω. This allows the use of low ESR chip capacitors.

The regulators are also suited for automotive applications, with built in protection from reverse battery connections, two-battery jumps and up to +60V/−50V load dump transients. Familiar regulator features such as short circuit and thermal shutdown protection are also built in.

Connection Diagrams

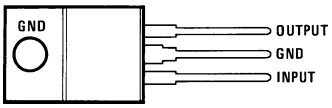


Figure 1. TO-220 Plastic Package
Front View
See Package Number NDE0003B

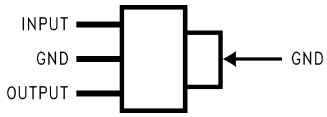


Figure 2. SOT-223 Plastic Package
Front View
See Package Number DCY0004A

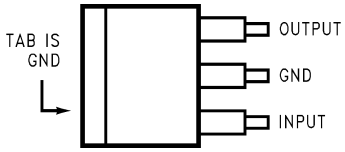


Figure 3. DDPAK/TO-263 Surface-Mount Package
Top View
See Package Number KTT0003B

Figure 4. DDPAK/TO-263 Surface-Mount Package
Side View
See Package Number KTT0003B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Input Voltage	Continuous	26V
	Transient (t ≤ 100 ms)	60V
Internal Power Dissipation (3)		Internally Limited
Maximum Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Soldering	TO-220 (10 seconds)	260°C
	DDPAK/TO-263 (10 seconds)	230°C
	SOT-223 (Vapor Phase, 60 seconds)	215°C
	SOT-223 (Infrared, 15 seconds)	220°C
ESD Susceptibility (4)		2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its rated Operating Conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation at any ambient temperature is $P_{MAX} = (125 - T_A)/\theta_{JA}$, where 125 is the maximum junction temperature for operation, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. If this dissipation is exceeded, the die temperature will rise above 125°C and the electrical specifications do not apply. If the die temperature rises above 150°C, the regulator will go into thermal shutdown. The junction-to-ambient thermal resistance θ_{JA} is 65°C/W, for the TO-220 package, 73°C/W for the DDPAK/TO-263 package, and 174°C/W for the SOT-223 package. When used with a heatsink, θ_{JA} is the sum of the device junction-to-case thermal resistance θ_{JC} of 3°C/W and the heatsink case-to-ambient thermal resistance. If the DDPAK/TO-263 or SOT-223 packages are used, the thermal resistance can be reduced by increasing the P.C. board copper area thermally connected to the package (see Application Hints for more information on heatsinking).
(4) ESD rating is based on the human body model, 100 pF discharged through 1.5 kΩ.

Operating Conditions(1)

Temperature Range (2)	LM2937ES, LM2937ET	$-40°C \le T_A \le 125°C$
	LM2937IMP	$-40°C \le T_A \le 85°C$
Input Voltage Range		4.75V to 26V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its rated Operating Conditions.
(2) The maximum allowable power dissipation at any ambient temperature is $P_{MAX} = (125 - T_A)/\theta_{JA}$, where 125 is the maximum junction temperature for operation, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. If this dissipation is exceeded, the die temperature will rise above 125°C and the electrical specifications do not apply. If the die temperature rises above 150°C, the regulator will go into thermal shutdown. The junction-to-ambient thermal resistance θ_{JA} is 65°C/W, for the TO-220 package, 73°C/W for the DDPAK/TO-263 package, and 174°C/W for the SOT-223 package. When used with a heatsink, θ_{JA} is the sum of the device junction-to-case thermal resistance θ_{JC} of 3°C/W and the heatsink case-to-ambient thermal resistance. If the DDPAK/TO-263 or SOT-223 packages are used, the thermal resistance can be reduced by increasing the P.C. board copper area thermally connected to the package (see Application Hints for more information on heatsinking).

Electrical Characteristics(1)

$V_{IN} = V_{NOM} + 5V$, I_{OUTmax} = 500 mA for the TO-220 and DDPAK/TO-263 packages, I_{OUTmax}=400mA for the SOT-223 package, C_{OUT} = 10 µF unless otherwise indicated. **Boldface limits apply over the entire operating temperature range, of the indicated device**, all other specifications are for $T_A = T_J$ = 25°C.

Output Voltage (V_{OUT})		2.5V		3.3V		Units
Parameter	**Conditions**	**Typ**	**Limit**	**Typ**	**Limit**	
Output Voltage	5 mA ≤ I_{OUT} ≤ I_{OUTmax}		2.42		3.20	V (Min)
		2.5	**2.38**	3.3	**3.14**	V(Min)
			2.56		3.40	V(Max)
			2.62		**3.46**	V(Max)
Line Regulation(2)	4.75V ≤ V_{IN} ≤ 26V, I_{OUT} = 5 mA	7.5	**25**	9.9	**33**	mV(Max)
Load Regulation	5 mA ≤ I_{OUT} ≤ I_{OUTmax}	2.5	**25**	3.3	**33**	mV(Max)
Quiescent Current	7V ≤ V_{IN} ≤ 26V, I_{OUT} = 5 mA	2	**10**	2	**10**	mA(Max)
	V_{IN} = (V_{OUT} + 5V), I_{OUT} = I_{OUTmax}	10	**20**	10	**20**	mA(Max)
	V_{IN} = 5V, I_{OUT} = I_{OUTmax}	66	100**125**	66	100**125**	mA(Max)
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 5 mA	75		99		µVrms
Long Term Stability	1000 Hrs.	10		13.2		mV
Short-Circuit Current		1.0	**0.6**	1.0	**0.6**	A(Min)
Peak Line Transient Voltage	t_f < 100 ms, R_L = 100Ω	75	**60**	75	**60**	V(Min)
Maximum Operational Input Voltage			**26**		**26**	V(Min)
Reverse DC Input Voltage	V_{OUT} ≥ −0.6V, R_L = 100Ω	−30	**−15**	−30	**−15**	V(Min)
Reverse Transient Input Voltage	t_r < 1 ms, R_L = 100Ω	−75	**−50**	−75	**−50**	V(Min)

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) The minimum input voltage required for proper biasing of these regulators is 4.75V. Below this level the outputs will fall out of regulation. This effect is not the normal dropout characteristic where the output falls out of regulation due to the PNP pass transistor entering saturation. If a value for worst case effective input to output dropout voltage is required in a specification, the values should be 2.37V maximum for the LM2937-2.5 and 1.6V maximum for the LM2937-3.3.

Typical Performance Characteristics

Output Voltage vs Temperature (2.5V)

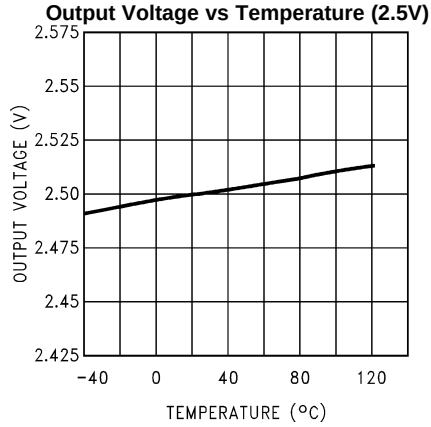


Figure 5.

Output Voltage vs Temperature (3.3V)

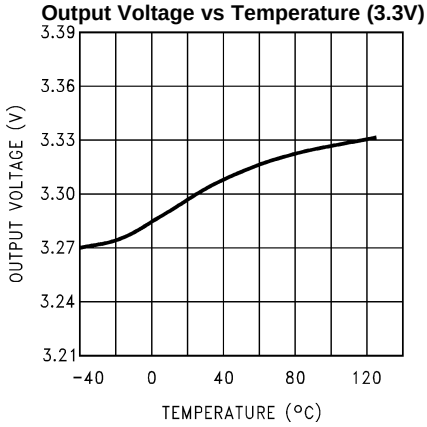


Figure 6.

Quiescent Current vs Output Current (2.5V)

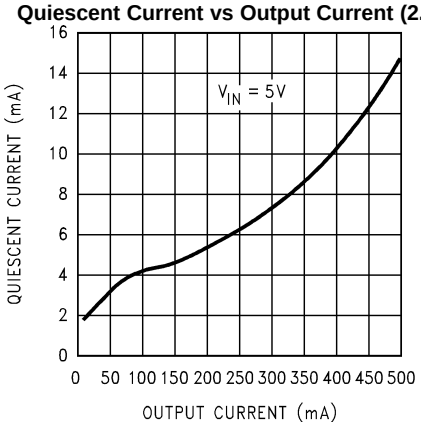


Figure 7.

Quiescent Current vs Output Current (3.3V)

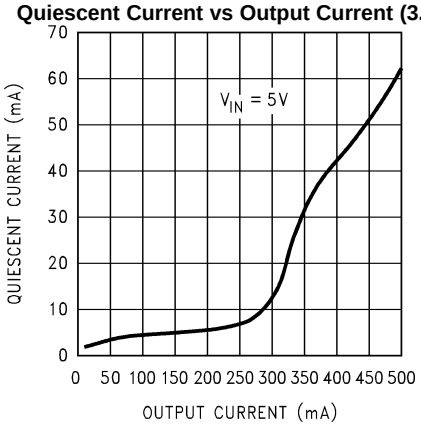


Figure 8.

Quiescent Current vs Input Voltage (2.5V)

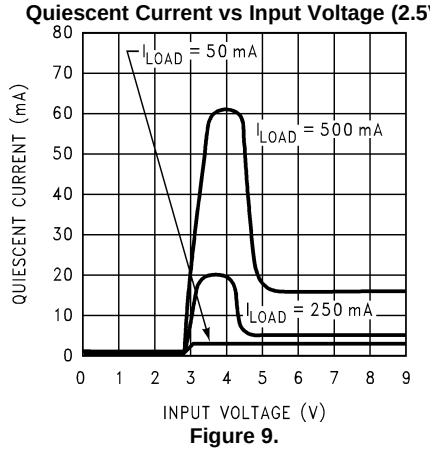


Figure 9.

Quiescent Current vs Input Voltage (3.3V)

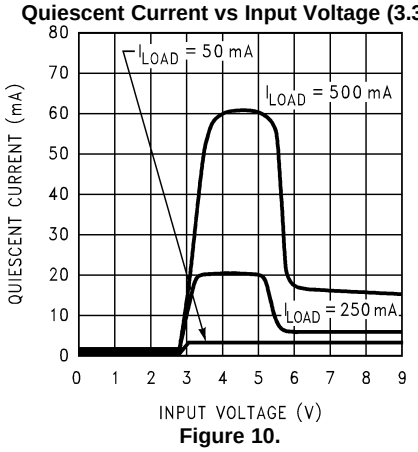


Figure 10.

Typical Performance Characteristics (continued)

Line Transient Response

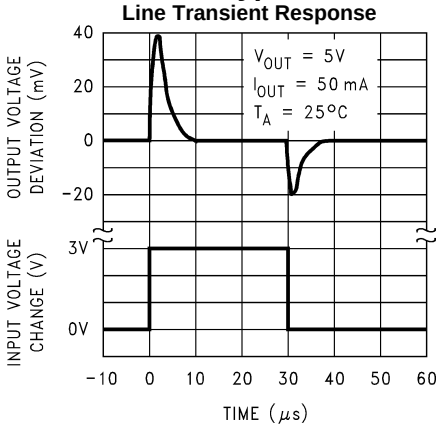


Figure 11.

Load Transient Response

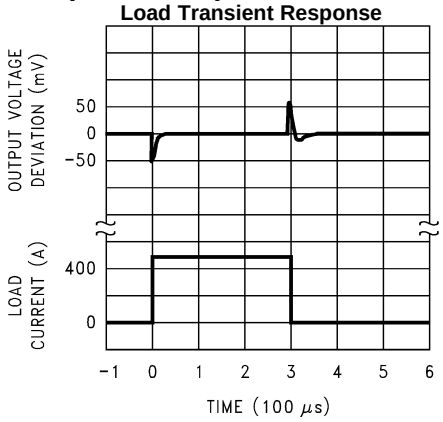


Figure 12.

Ripple Rejection

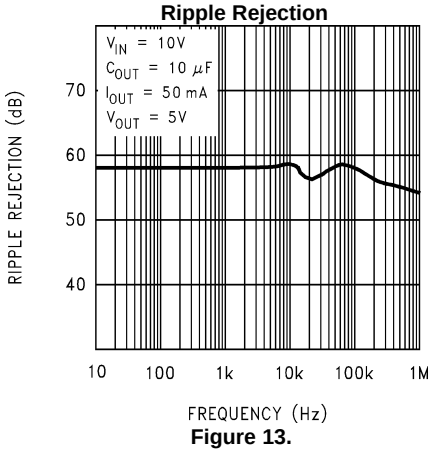


Figure 13.

Output Impedance

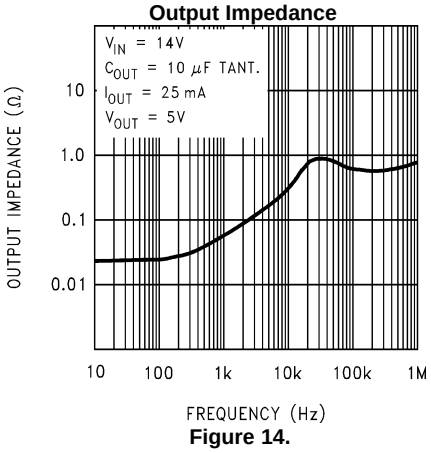


Figure 14.

Maximum Power Dissipation (TO-220)

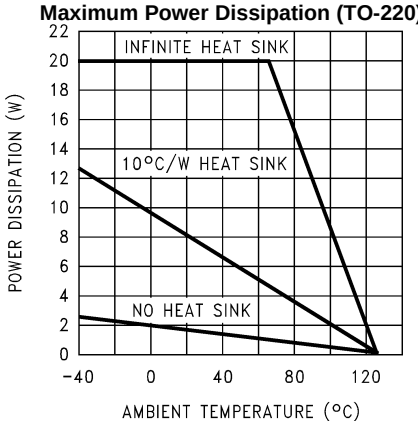


Figure 15.

Maximum Power Dissipation (DDPAK/TO-263) (1)

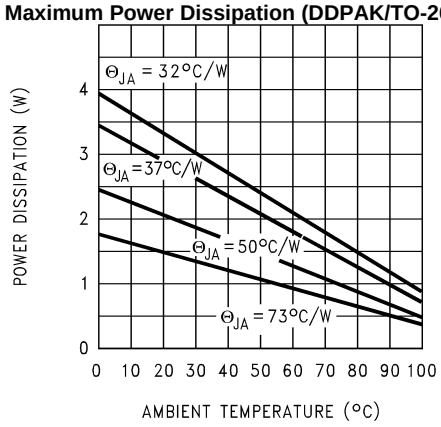


Figure 16.

(1) The maximum allowable power dissipation at any ambient temperature is $P_{MAX} = (125 - T_A)/\theta_{JA}$, where 125 is the maximum junction temperature for operation, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. If this dissipation is exceeded, the die temperature will rise above 125°C and the electrical specifications do not apply. If the die temperature rises above 150°C, the regulator will go into thermal shutdown. The junction-to-ambient thermal resistance θ_{JA} is 65°C/W, for the TO-220 package, 73°C/W for the DDPAK/TO-263 package, and 174°C/W for the SOT-223 package. When used with a heatsink, θ_{JA} is the sum of the device junction-to-case thermal resistance θ_{JC} of 3°C/W and the heatsink case-to-ambient thermal resistance. If the DDPAK/TO-263 or SOT-223 packages are used, the thermal resistance can be reduced by increasing the P.C. board copper area thermally connected to the package (see Application Hints for more information on heatsinking).

Typical Performance Characteristics (continued)

Low Voltage Behavior (2.5V)

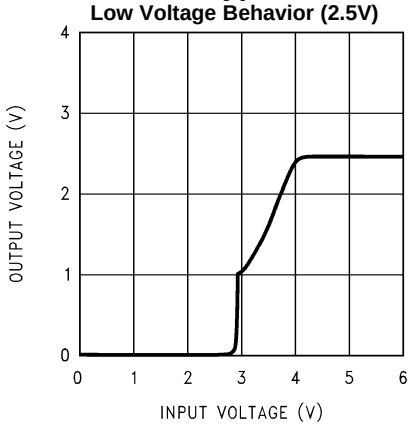


Figure 17.

Low Voltage Behavior (3.3)

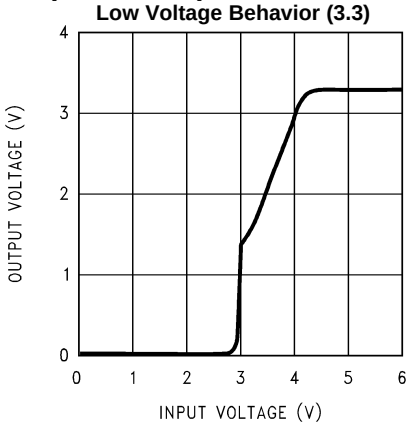


Figure 18.

Output at Voltage Extremes

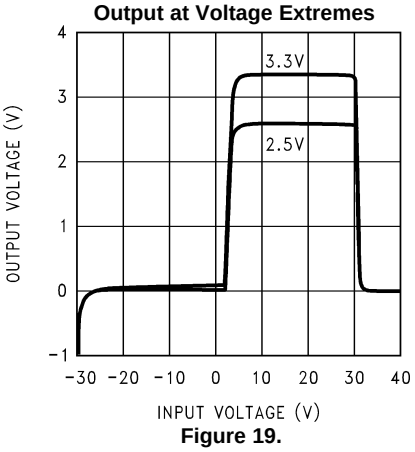


Figure 19.

Output Capacitor ESR

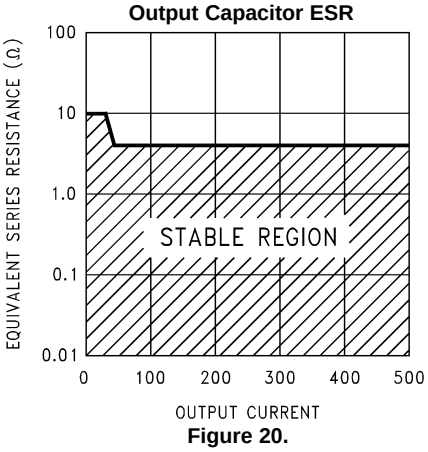


Figure 20.

Peak Output Current

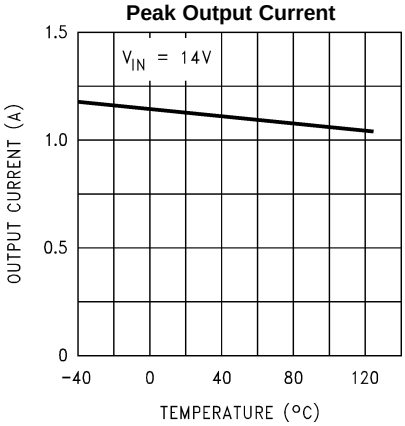
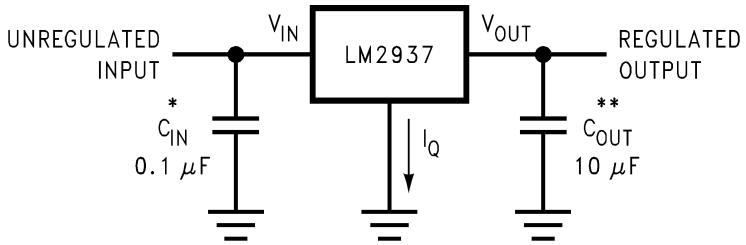


Figure 21.

Typical Application



* Required if the regulator is located more than 3 inches from the power supply filter capacitors.
** Required for stability. C_{out} must be at least 10 μF (over the full expected operating temperature range) and located as close as possible to the regulator. The equivalent series resistance, ESR, of this capacitor may be as high as 3Ω

APPLICATION HINTS

EXTERNAL CAPACITORS

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR (Equivalent Series Resistance) and minimum amount of capacitance.

MINIMUM CAPACITANCE:

The minimum output capacitance required to maintain stability is 10 μF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

ESR LIMITS:

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in the graph below. ***It is essential that the output capacitor meet these requirements, or oscillations can result.***

Figure 22. Output Capacitor ESR

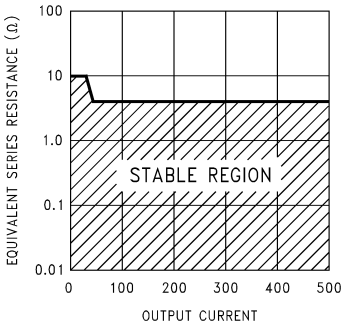


Figure 23. ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to −40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid Tantalum, with the total capacitance split about 75/25% with the Aluminum being the larger value.

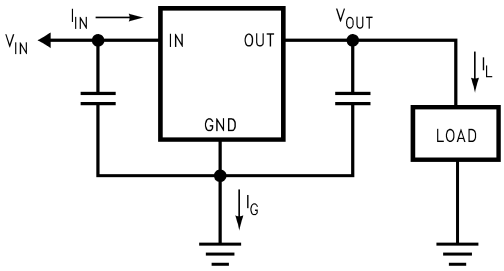
If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The “flatter” ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

The figure below shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



$I_{IN} = I_L \div I_G$
$P_D = (V_{IN} - V_{OUT})\ I_L + (V_{IN})\ I_G$

Figure 24. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R (max). This is calculated by using the formula:

$T_R\ (max) = T_J(max) - T_A\ (max)$

where:

- T_J (max) is the maximum allowable junction temperature, which is 125°C for commercial grade parts.
- T_A (max) is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for T_R(max) and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$\theta_{(J-A)} = T_R\ (max)/P_D$

NOTE

If the maximum allowable value for $\theta_{(J-A)}$ is found to be ≥ 53°C/W for the TO-220 package, ≥ 80°C/W for the DDPAK/TO-263 package, or ≥174°C/W for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for $\theta_{(J-A)}$falls below these limits, a heatsink is required.

HEATSINKING TO-220 PACKAGE PARTS

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{(J-A)}$ will be the same as shown in the next section for the DDPAK/TO-263.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, $\theta_{(H-A)}$, must first be calculated:

$\theta_{(H-A)} = \theta_{(J-A)} - \theta_{(C-H)} - \theta_{(J-C)}$

Where:

- $\theta_{(J-C)}$ is defined as the thermal resistance from the junction to the surface of the case. A value of 3°C/W can be assumed for $\theta_{(J-C)}$ for this calculation.
- $\theta_{(C-H)}$ is defined as the thermal resistance between the case and the surface of the heatsink. The value of $\theta_{(C-H)}$ will vary from about 1.5°C/W to about 2.5°C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2°C/W should be assumed for $\theta_{(C-H)}$.

When a value for $\theta_{(H-A)}$ is found using the equation shown, *a heatsink must be selected that has a value that is less than or equal to this number.*

$\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

HEATSINKING DDPAK/TO-263 AND SOT-223 PACKAGE PARTS

Both the DDPAK/TO-263 ("KTT") and SOT-223 ("DCY") packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 25 shows for the DDPAK/TO-263 the measured values of $\theta_{(J-A)}$ for different copper area sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking.*

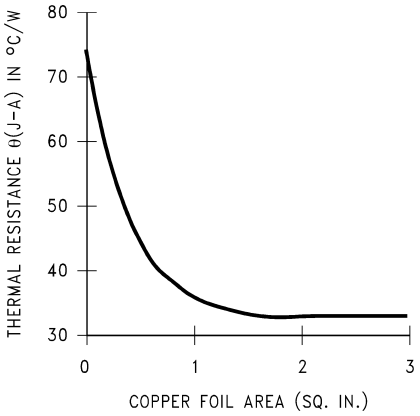


Figure 25. $\theta_{(J-A)}$ vs Copper (1 ounce) Area for the DDPAK/TO-263 Package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(J-A)}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

As a design aid, Figure 26 shows the maximum allowable power dissipation compared to ambient temperature for the DDPAK/TO-263 device (assuming $\theta_{(J-A)}$ is 35°C/W and the maximum junction temperature is 125°C).

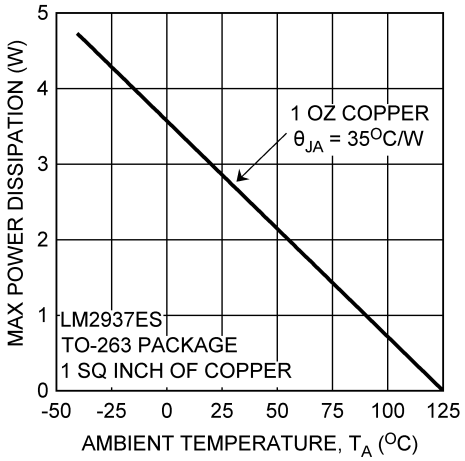


Figure 26. Maximum Power Dissipation vs T_{AMB} for the DDPAK/TO-263 Package

Figure 27 and Figure 28 show the information for the SOT-223 package. Figure 28 assumes a $\theta_{(J-A)}$ of 74°C/W for 1 ounce copper and 51°C/W for 2 ounce copper and a maximum junction temperature of +85°C.

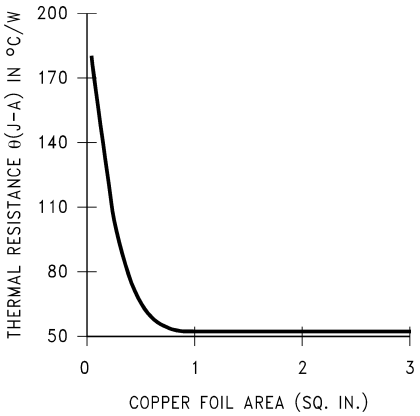


Figure 27. $\theta_{(J-A)}$ vs Copper (2 ounce) Area for the SOT-223 Package

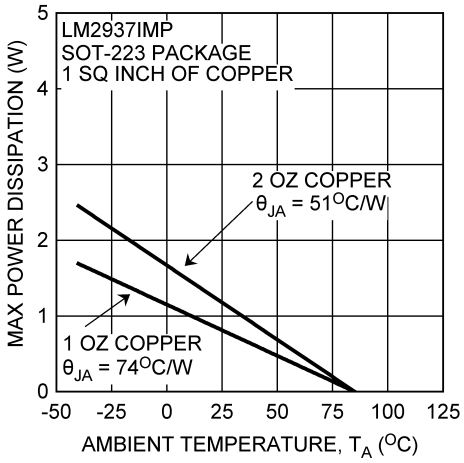


Figure 28. Maximum Power Dissipation vs T_{AMB} for the SOT-223 Package

Please see AN-1028 (SNVA036) for power enhancement techniques to be used with the SOT-223 package.

SOT-223 SOLDERING RECOMMENDATIONS

It is not recommended to use hand soldering or wave soldering to attach the small SOT-223 package to a printed circuit board. The excessive temperatures involved may cause package cracking.

Either vapor phase or infrared reflow techniques are preferred soldering attachment methods for the SOT-223 package.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2937ES-2.5	NRND	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2937ES -2.5	
LM2937ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2937ES -2.5	Samples
LM2937ES-3.3	NRND	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2937ES -3.3	
LM2937ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2937ES -3.3	Samples
LM2937ESX-3.3	NRND	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM2937ES -3.3	
LM2937ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2937ES -3.3	Samples
LM2937ET-2.5	NRND	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2937ET -2.5	
LM2937ET-2.5/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2937ET -2.5	Samples
LM2937ET-3.3	NRND	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2937ET -3.3	
LM2937ET-3.3/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2937ET -3.3	Samples
LM2937IMP-2.5	NRND	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L68B	
LM2937IMP-2.5/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L68B	Samples
LM2937IMP-3.3	NRND	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L69B	
LM2937IMP-3.3/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L69B	Samples
LM2937IMPX-2.5/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L68B	Samples
LM2937IMPX-3.3	NRND	SOT-223	DCY	4	2000	TBD	Call TI	Call TI	-40 to 85	L69B	
LM2937IMPX-3.3/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L69B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

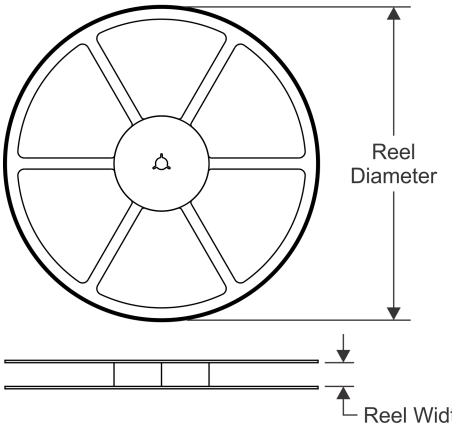
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

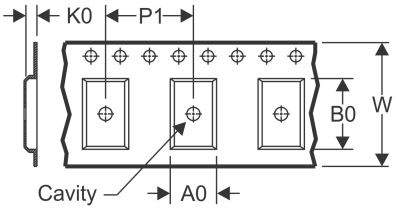
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

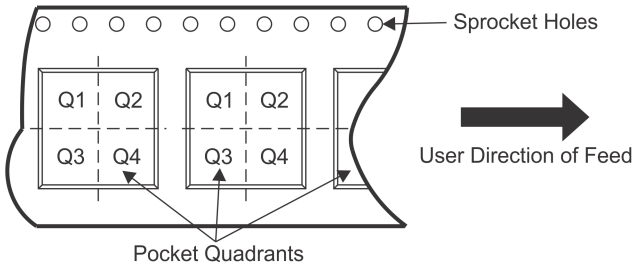


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

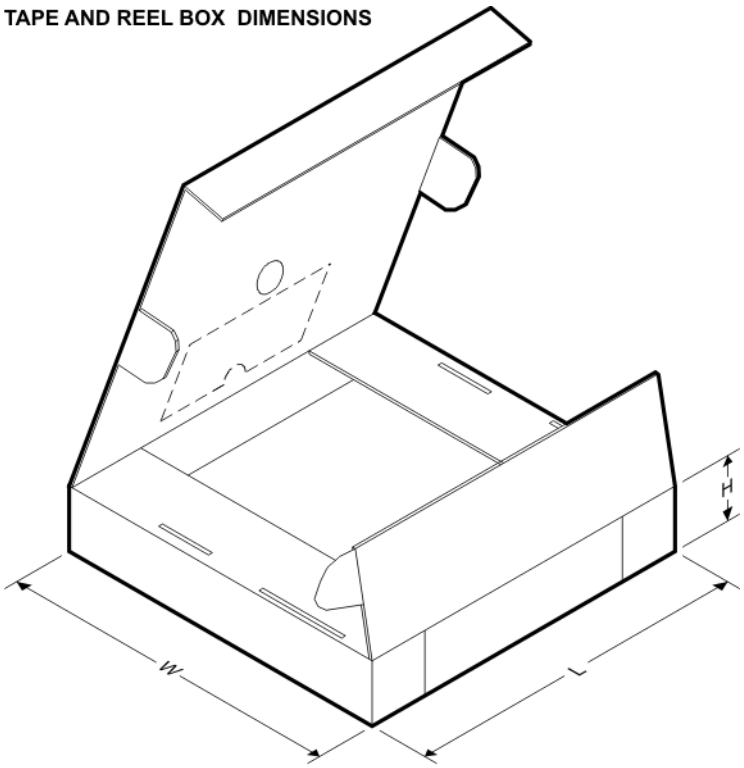
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2937ESX-3.3	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2937ESX-3.3/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2937IMP-2.5	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2937IMP-2.5/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2937IMP-3.3	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2937IMP-3.3/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2937IMPX-2.5/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2937IMPX-3.3	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM2937IMPX-3.3/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3

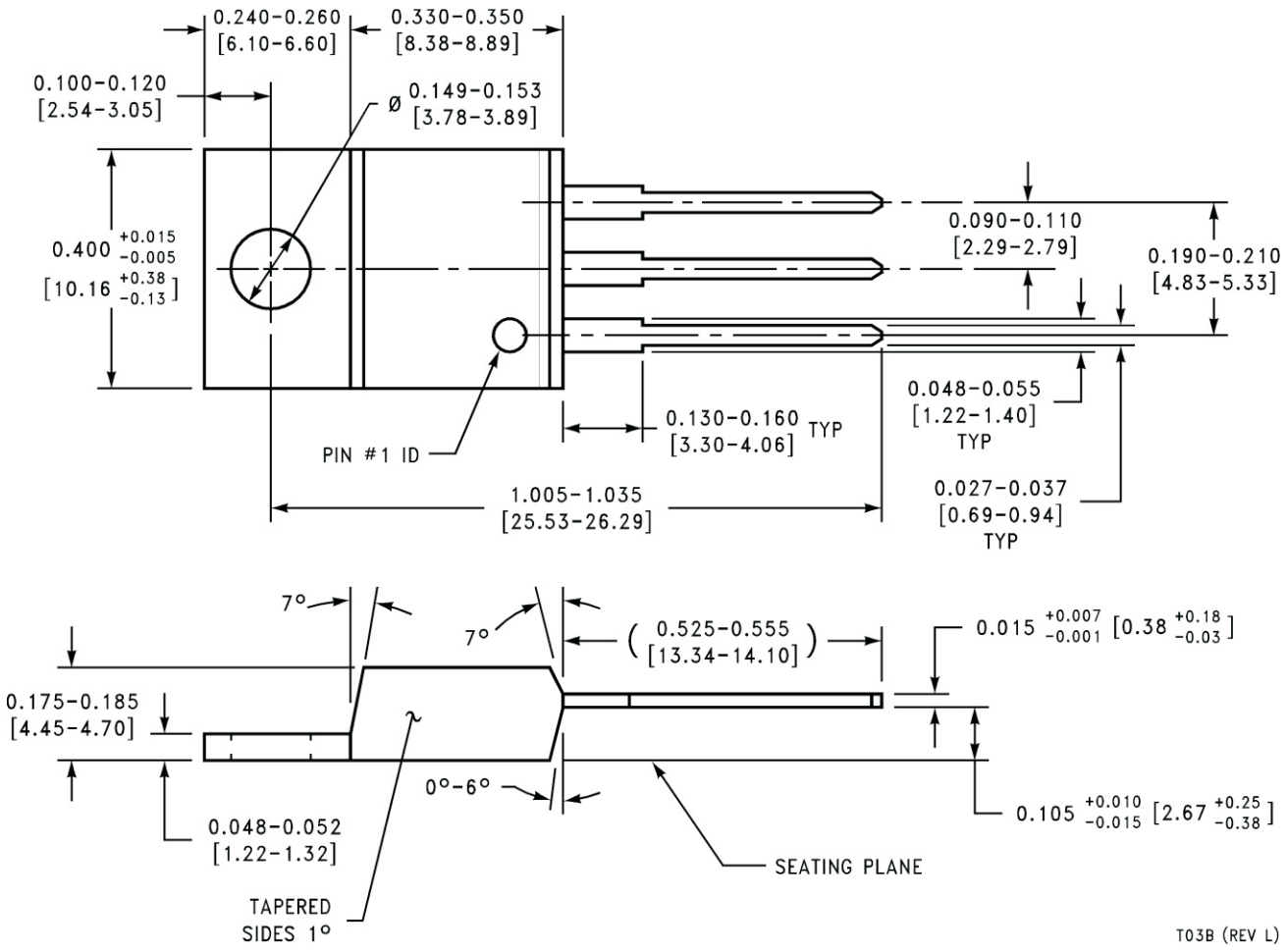
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

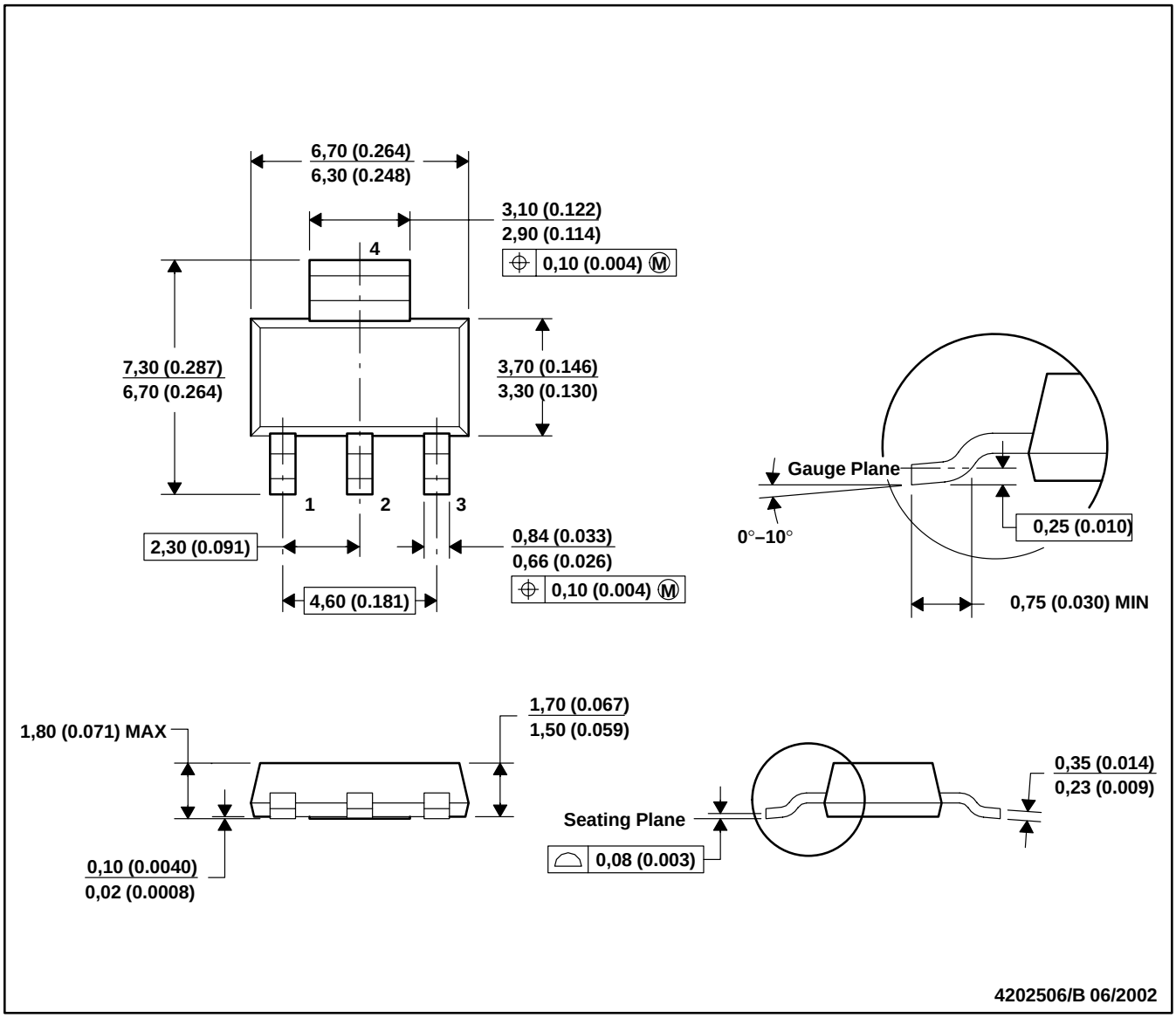
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2937ESX-3.3	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM2937ESX-3.3/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM2937IMP-2.5	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2937IMP-2.5/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2937IMP-3.3	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2937IMP-3.3/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM2937IMPX-2.5/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2937IMPX-3.3	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM2937IMPX-3.3/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0

NDE0003B


0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
0.090-0.110
[2.29-2.79]
0.190-0.210
[4.83-5.33]
PIN #1 ID
0.130-0.160 TYP
[3.30-4.06]
0.048-0.055
[1.22-1.40]
TYP
1.005-1.035
[25.53-26.29]
0.027-0.037
[0.69-0.94]
TYP
7°
7°
(0.525-0.555
[13.34-14.10])
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185
[4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052
[1.22-1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

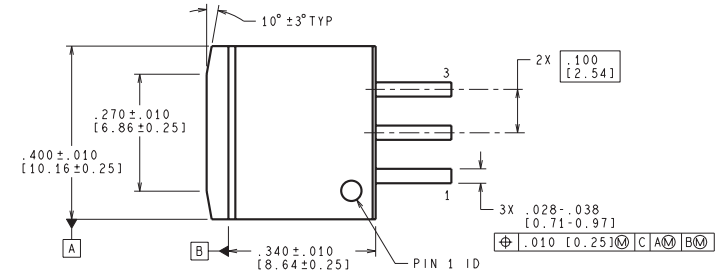
MPDS094A – APRIL 2001 – REVISED JUNE 2002

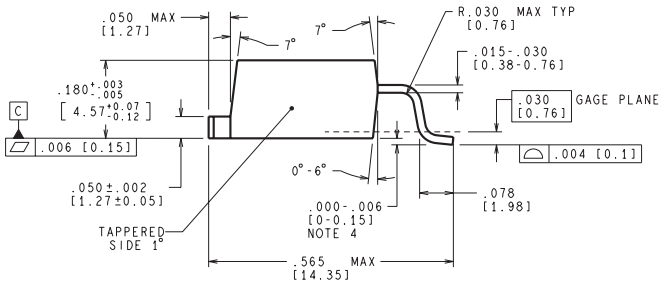
DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**

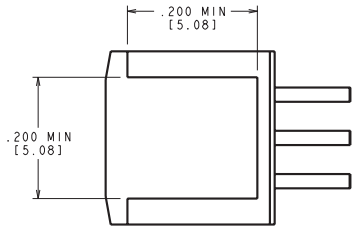


NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

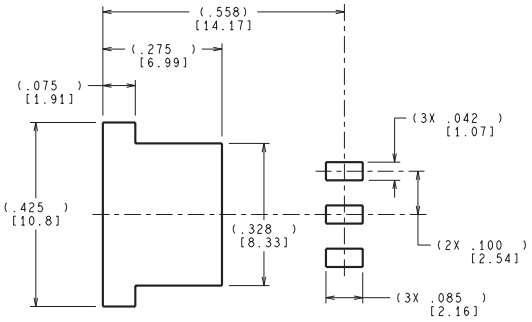
KTT0003B







BOTTOM SIDE OF PACKAGE



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VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS3B (Rev F)

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